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Using Charge Coupled Devices Can Reduce Bulk Memory Costs

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CCD's offer adequate performance in these applications and provide truly significant cost savings when compared to RAM configurations.

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Over the course of the past several years, semiconductor memories have become a dominant form of main memory. And today they are being applied in secondary or bulk storage applications as well. Assuming that you've already made the decision to go semiconductor for your bulk storage, the first and most important choice facing you is this—should you go the MOS RAM (Random Access Memory) or CCD memory component route?

In areas where their performance is adequate, CCD memories can provide a significant reduction in cost for bulk memory applications. At both the component and system level, costs will be reduced by 65 to 75% by using CCD's instead of RAM's.

Quite naturally, such significant savings have not gone unnoticed and many systems have been configured to take advantage of the favorable CCD cost picture. We contend that these savings will always be possible. By their very nature, CCD's require simpler design techniques and offer both higher densities and higher yields than RAM's. The result is lower manufacturing costs both today and in the future because any advances in manufacturing or photolithography techniques will equally benefit both CCD and RAM technologies.

You can find all the answers inside

Understanding actual device costs requires some understanding of device construction and

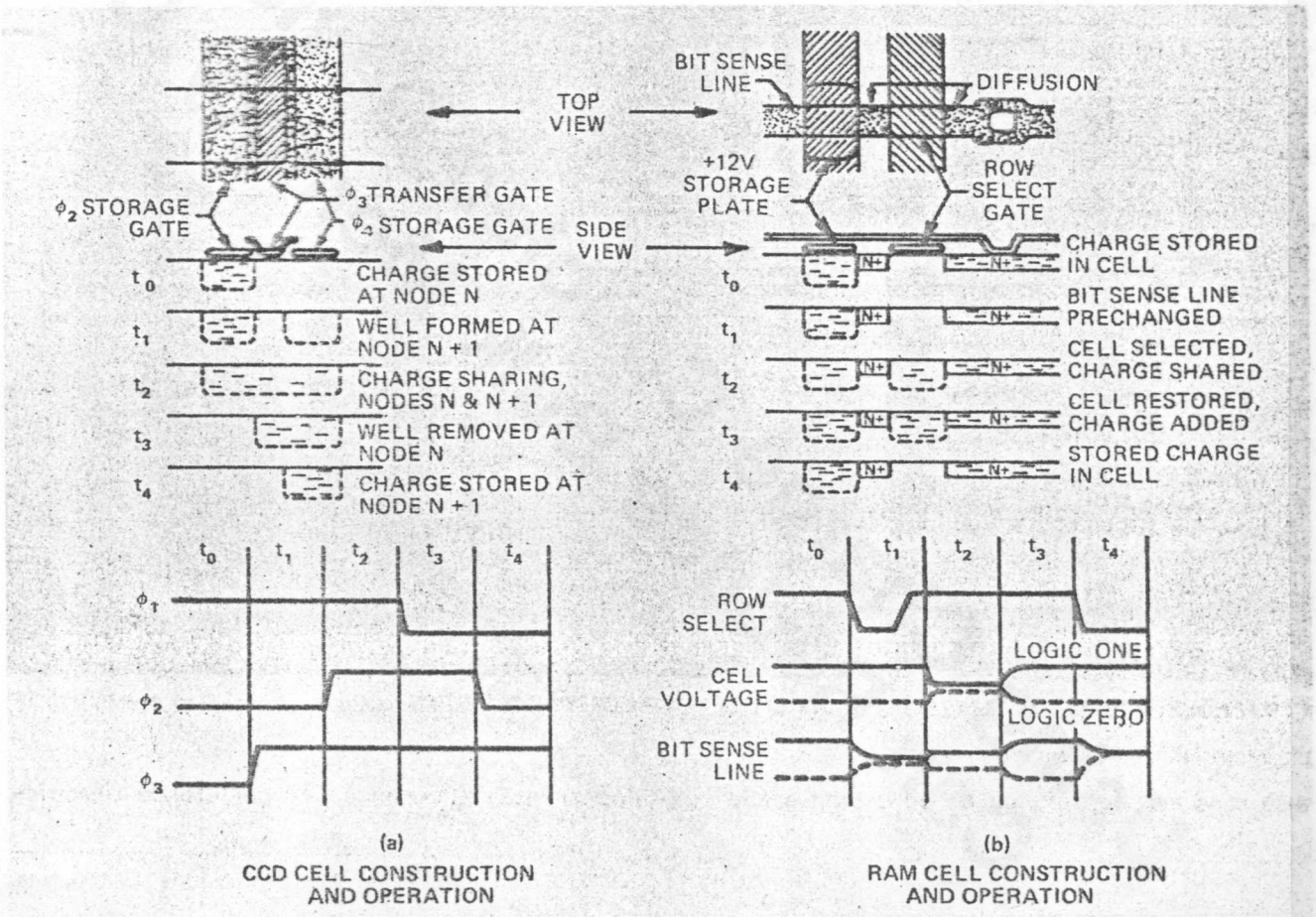

Fig. 1—Identical storage methods are employed in both the CCD and RAM cells. The positive electrode under which charge is stored is clocked in a CCD, rather than tied to a positive voltage as in the RAM.

operation. **Fig. 1** shows the basic construction of a storage cell from a 4-phase surface-channel CCD and a single transistor cell dynamic RAM. Note that in both cases the storage method is the same—charge storage in a depletion region under a positively charged electrode. Disposition of this electrode varies, however, being tied to +12V in a RAM, and clocked in CCD's. Charge transfer performs storage cell access, accomplished by turning on a MOS device to connect the storage node to either the next storage cell (CCD) or a bit sense line (RAM).

Dynamic RAM charge transfer, a generally well understood function, occurs as follows: An X or row decoder gates one transfer device per bit sense line, passing information from that cell onto the precharged bit sense line. A small positive shift occurs on the bit sense line if charge was stored in the cell; a small negative shift, if no charge was stored. In order to rewrite the data in the cell, this small shift in bit sense line voltage must be amplified by the sense amplifier.

The information transfer method in a CCD is generally not as well known, even though the mechanism is very similar and quite simple. Appropriate sequencing of a series of shift clocks common to each cell within a loop controls charge transfer. For example, the 2416, a 16k CCD available on the market today, uses four clocks, each tied to all loops. Other configurations are possible, however.

Right-left or left-right—how goes the flow?

Because the CCD is itself symmetrical to charge flow, charge can be moved either left-to-right or right-to-left, depending on the sequencing of the clocks. Most designs, however, restrict the flow of charge to one direction to simplify the design of the refresh amplifier within a loop.

Fig. 1a shows a charge packet—representing a logic ONE—moving one location to the right as the clocks are sequenced. A well first forms at node n+1 when phase 4 goes HIGH. But it contains no charge until transfer phase 3 connects the charge at node n to the well at node n+1, causing redistribution of the charge over the larger storage well. Transfer completes as phase 2 and then phase 3 go LOW, causing the well to shorten and the charge to flow to the n+1 node. A logic ZERO transfers in the same fashion, except the charge packet contains significantly less charge.

Let's get organized

The primary organizational difference between a RAM and a CCD is that the RAM—because of its direct access capability—requires a very long and highly capacitive bit sense line to conduct the stored charge to the sense amplifier. In contrast, a CCD moves the charge serially to a sense amplifier at the end of a register. This charge dumps onto a low capacitance region, resulting in significantly larger voltage transitions than experienced with RAM's. For this reason, CCD sense amplifiers can be greatly simplified. In turn, since sense amplifiers represent a major portion of RAM power dissipation, RAM's use considerably more power than CCD's.

Fig. 2 shows the layout of a 16k dynamic RAM and a 16k CCD. Because of the additional decoders required, the more complex sense amplifiers, and the increased timing and control, the RAM-cell periphery represents 66% of the total chip area. This compares to 45% for the CCD.

Although these organizational factors tend to lower CCD manufacturing costs somewhat, the primary cost differences tend to relate to the simpler construction techniques for the CCD storage array. In **Fig. 1,** note that unlike the RAM design, the CCD cell has no metal-to-silicon contacts, requires no diffusions and contains no metal. The CCD array is an undisturbed area of silicon with overlaying gate structures.

Device costs reflect device complexity

These fabrication advantages combine to produce a price per bit ratio between RAM's and CCD's of approximately 4:1; i.e., a 16k CCD costs about the same at the device level as the 4k RAM. But while this price ratio exists today for comparable quantities and deliveries, will it continue in the future? The fact that both RAM's and CCD's

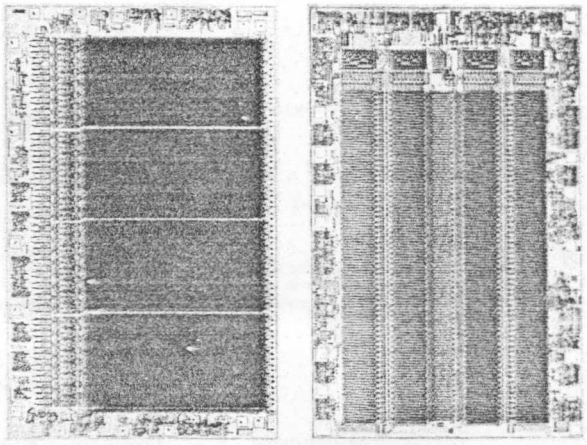

Fig. 2—Lower manufacturing costs are the direct result of CCD chip organizational factors. As the comparison shows, almost half again as much of the RAM chip area is dedicated to peripheral circuit requirements (decoders, amplifiers, etc.).

TABLE 1
BOARD COST–CCD vs. RAM

	16k CCD				4k RAM				16k RAM			
	QTY.	ITEM	COST	TOTAL	QTY.	ITEM	COST	TOTAL	QTY.	ITEM	COST	TOTAL
STORAGE DEVICES	64	2416	$8	$512	64	2104	$8	$512	64	2116	$32	$2048
CLOCK DRIVERS	16	5244	$3	$ 48	2	TTL	$0.5	$ 1	2	TTL	$0.5	$ 1
OTHER MEMORY DRIVERS	6	3245	$3	$ 18	6	TTL	$0.5	$ 3	6	TTL	$0.5	$ 3
LOGIC	10	TTL	$0.5	$ 5	10	TTL	$0.5	$ 5	10	TTL	$0.5	$ 5
P.C. BOARDS	1	PCB	$35	$ 35	1	PCB	$35	$ 35	1	PCB	$35	$ 35
MISC. COMPONENTS			$10	$ 10			$10	$ 10			$10	$ 10
ASSEMBLY & TEST			$60	$ 60			$60	$ 60			$60	$ 60
TOTAL				$688				$626				$2162

are currently available in 16k densities prompts some concern that the ratio has already collapsed, even though 16k CCD's have been in production for two years and 16k RAM's are just entering early production. To understand why this is not the case, let's study historical MOS trends.

Using the past to predict the future

From the introduction of the integrated flip-flop to the 16k dynamic RAM, the trend has been that RAM densities increase by a factor of four every two years. Dynamic RAM's have led the way, with static RAM's following one generation (two years) behind. Fabrication similarities for dynamic RAM's and CCD's, coupled with the more simplified CCD cell and array structure, suggest that a given density can be achieved at an earlier point in time with a CCD organization than with a RAM organization. Actually, CCD devices appear to be one year (one half a generation) ahead of RAM devices in level of integration.

A corollary of the previously mentioned postulate (i.e., a factor of four increase in density every two years) states that a factor of two reduction in price/bit is achieved with every new level of density. That is, two years gives a factor of four in density and a factor of one half in price/bit. These trends have been maintained through many successive generations of devices. At each generation, the new device is initially manufactured and sold at a cost/bit premium over the previous generation. Early in the product life, cost falls rapidly as the new device moves into full production. Typically, within a year the cost drops below the level established by the previous device, eventually tending towards a level of approximately one half the previous bit cost.

Technology transfers back and forth

One factor supporting the continuation of a constant price ratio between CCD's and RAM's relates to the close similarities in their fabrication. The relationship between CCD development and dynamic RAM development is more causal than it appears. In fact, it was the development of the 4k RAM that led to the development of the 16k CCD, that in turn led to the development of the 16k RAM.

Next generation devices build on current generation technology, and in this way shipments of either CCD's or RAM's provide a learning experience for the process, and both device types benefit. Any improvements in masking technology made for RAM's or CCD's can be applied to the other. Similarly, any reduction in defect densities made for one reduces the defect density for the other. Thus, the RAM and CCD share a joint learning curve.

The numbers tell the story

Now for a specific example—a hypothetical 10M-byte bulk storage system. To compare currently available 16k CCD's and 4k RAM's would somewhat distort the analysis due to the half generation difference between CCD and RAM developments. Therefore, we have also included 16k RAM's in the analysis, although 16k RAM availability lags 16k CCD availability by about one year.

A 8-in. × 12-in. board can hold 64 storage devices with their associated drivers. **Table 1** compares the cost of such a memory board incorporating CCD or RAM devices, with the assumed device costs based on medium volume

TABLE 2
STRUCTURAL, ASSEMBLY AND TEST COSTS

	16k CCD/RAM			4k RAM		
	QTY.	COST	TOTAL	QTY.	COST	TOTAL
CHASSIS & BACKPLANE	3	400	1200	10	400	4000
MAINTENANCE PANEL	1	500	500	1	500	500
CABLING			500			1000
CABINET			500			1000
SYSTEM ASSEMBLY			1000			2000
SYSTEM TEST			1000			1500
TOTAL			$4700			$10,000

TABLE 3
SYSTEM COST-CCD vs. RAM

	16k CCD			4k RAM			16k RAM		
	QTY.	COST	TOTAL	QTY.	COST	TOTAL	QTY.	COST	TOTAL
STORAGE BOARDS	80	668	55,040	320	626	200,320	80	2162	172,960
CONTROL UNIT	1	700	700	1	700	700	1	500	500
POWER SUPPLY	1kW	$1/W	1,000	2kW	$1/W	2,000	0.7kW	$1/W	700
STRUCTURAL, ASS'Y & TEST			4,700			10,000			4,700
TOTAL			$61,440			$213,020			$178,860

TABLE 4
BIT COST COMPARISON—CCD vs. RAM

	16k CCD		4k RAM		16k RAM	
	COST (m¢/BIT)	%	COST (m¢/BIT)	%	COST (m¢/BIT)	%
STORAGE DEVICES	48.8	66.7	195.3	76.9	195.3	91.6
CLOCK DRIVERS	4.6	6.3	0.4	0.1	0.1	–
OTHER BOARD COSTS	12.2	16.7	43.1	17.0	10.8	5.1
CONTROL UNIT	0.8	1.1	0.8	0.3	0.6	0.3
POWER	1.2	1.6	2.4	1.0	0.8	0.4
STRUCTURAL, ASS'Y & TEST	5.6	7.6	11.9	4.7	5.6	2.6
TOTAL	73.2		253.9		213.2	

purchases of standard products. Higher volumes would produce lower prices, but would not disturb the price ratios and would not materially affect the results of the comparison.

The CCD board requires 16 MOS-level drivers for the CCD shift clock inputs, compared to two TTL-level clock drivers for the RAM's. It also needs MOS-level address and control drivers instead of TTL-level drivers. The remaining board costs are the same.

A chassis 22-in. W×9-in. H×13-in. D holds 32 memory boards spaced 5/8 in. apart. Three chassis hold the 80 16k CCD or 16k RAM boards required for the complete system with room to spare. By contrast, you need ten chassis to hold the 320 4k RAM boards for this size system.

Table 2 breaks out structural, assembly and t costs. Although these are identical for the 1 CCD and 16k RAM systems, they are considera higher for the 4k RAM system due to the lar number of boards and components. **Table** summarizes all system costs. The hypotheti 10M byte system costs $61,440 when built w CCD's, or $117,420 less than the least expens (16k) RAM system.

Observe that the 4:1 RAM/CCD device c ratio reduces to a 3:1 system cost ratio because the allocation of the other system costs to memory as shown in **Table 4.** Notice also that d 67% of the total CCD system cost is in the stor devices, compared to 92% for the 16k R system. □

Authors' biographies

Dave House is manager of Product Marketing and Applications at the Components Div. of Intel Corp. in Santa Clara, CA. In addition to running these two departments, Dave also gets involved in product planning, pricing and advertising. He has authored company application notes and contributed inputs to the Intel Memory Design Handbook. When he can find some spare time, Dave enjoys skiing, racketball and cycling.

Kirk MacKenzie is a CCD Product Marketing engineer at the Intel's Components Div. His present duties involve both product management and planning for CCD's as well as static RAM's. He has a BSEE from the Univ. of California and is presently working on his MBA. Kirk's hobbies incl photography, kayaking and backpacking.